interposing at least one conductive pattern between at least one pair of insulation layers so as to be in contact with at least one of the pair of insulation layers; and

forming a conductive coil,

wherein the interposing step includes electroforming at least one conductive pattern, and no specific gap is formed between the conductive pattern and the pair of insulation layers [has a thickness of 10 $\mu$m or more and a width to thickness ratio from 1 to less than 5].

17. The lamination chip inductor according to claim 16, wherein the conductive pattern has a width in the range from about 30 $\mu$m to about 70 $\mu$m, and a thickness in the range from about 20 $\mu$m to about 50 $\mu$m.

18. A lamination ceramic chip inductor, formed by the process comprising the steps of:

forming a conductive coil by electroforming at least one conductive pattern;

interposing said at least one conductive pattern between at least one pair of insulation layers so as to be in contact with at least one of the pair of insulation layers;

laminating the conductive coil between said at least one pair of insulation layers to form an integral body; and

sintering the integral body to form said lamination chip inductor;

whereby in the lamination ceramic chip inductor no specific gap is formed at interfaces between the conductive pattern and said insulation layers when the integral body is sintered.

19. The lamination ceramic chip inductor of claim 18, wherein the width of said conductive pattern is in the range from about 30 micrometers to about 70 micrometers